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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,301	08/28/2003	Thomas L. Drabenstott	800.0128	6929

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EXAMINER

PAN, DANIEL H

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N . 10/650,301	Applicant(s) DRABENSTOTT ET AL.	
	Examiner Daniel Pan	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 October 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) See Continuation Sheet is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 25-33, 58, 60-62, 64, 66-71, 73-75 and 77-79 is/are rejected.
- 7) ☒ Claim(s) 63 and 65 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Continuation of Disposition of Claims: Claims pending in the application are 25-33,60-68,70,73-75 and 77-79 (1-24, 34-35, 56,57,59,69,71,72,76 have been canceled).

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1. Claims 1-24, 34-35, 56,57,59,69,71,72,76 have been canceled. Claims 25-33, 60-68, 70, 73-75,77-79 remain for examination.

2. Upon further review and consideration, and based on the newly amended claims (claims 25,60,66, 73), the following action is in effect. Since claim 60 included the previously objected features, and now it has been rejected based on a new ground, the following is a non-final rejection to let applicant a chance to respond. The Office action supercedes the previous office action on 07/29/04.

Okayama et al. (5,684,728) is a newly cited art, and copy is attached with this Office action.

Fernando (5,802,360) was cited in a previous Office action, therefore, copy of this patent is not provided herein.

3. Applicant's arguments filed on 10/20/04 with respect to claims 25, 60,66,73 have been considered but are moot in view of the new ground(s) of rejection.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 25-33, 58, 60-62, 64,66-71, 73-75, 77-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fernando (5,802,360) in view of Okayama et al. (5,684,728) .
5. As to claims 25,66, Fernando disclosed at least :
 - a) defining a set of condition flags (see the PSW bits in col.4, lines 35-56);
 - b) specifying a condition code within a first instruction [eq0], executing the first instruction (see the extension to the instructions in col.4, lines 56-64, see also col.4, lines 56-61, col.5, lines 1-6 for additional instructions);
 - c) updating the condition flags upon the specified condition code [eq] and side effect [0] resulting from the execution of the first instruction (see the set flag upon eq0 in col.4, lines 63-64);
 - d) determining whether to execute the second instruction based on the condition flags (see the true and false determination for executing the branching or for adding and subtracting instructions in col.5, lines 7-20);
 - e) executing the second instructions (see the execution of the instruction based on the true or false in col.5, lines 7-20);
 - f) executing a first instruction , the first instruction having one or more bits to indicate how [eq] to set condition flag (see the instruction extension to set the flag in col.4, lines 53-64);
 - g) means for setting condition flags based on the one or more bits and the side effect [0] by execution of the first instruction (see the one of the first instructions in col.4, lines 56-64);

h) means for execution g a second instruction if determined (see the true and false determination for the next execution in col.5, lines 7-20).

6. Fernando did not specifically show his set of condition flags (see the PSW) was arithmetic flags as claimed. However, Okayama disclosed clearly a PSW for storing arithmetic flags (see the fig. PSW for storing overflow , carry). It would have been obvious to one of ordinary skill the art to use Okayama in Fernando for including arithmetic flags into the PSW because the use of Okayama could expand the capability of Fernando to adapt to specific application of the processor, such as the arithmetic conditional flags resulted from the arithmetic unit, and because Fernando also taught the flag in his PSW was modified by arithmetic instructions (see the flag modified by the multiply or division instructions in col.4, lines 57-67, col.5, lines 1-56), therefore one of ordinary skill in the art should be able to recognize the PSW of Fernando should be applicable for using the arithmetic flags in order to enhance the processing ability of the system ,and in doing so , provided a motivation.

7. As to claim 26, Fernando also combining the previous state with the result of the condition test (see the feedback flag combined with the new flag in fig.4).

8. As to claim 27, Fernando also included greater than and equal to (e.g. see col.4, lines 53-65).

9. As to claim 28, Fernando also tested the two operands (e.g. see col.2, line 55 , the compare test, see also other tests in col.4, lines 56-63).

10. As to claim 29, Fernando's compare instruction [CMP.eq r1, \$0] was also used to specify data type [\$]) (see the \$ parameter for specifying the numerical data type in col.2, line 55).

11. AS to claim 30, Fernando's also included Boolean combination (see CMP.eq, see also col.2, lines 1-11 for the background of combinatorial logic).

12. As to claim 31, Fernando's also including the branching in sequence processor (see the branch in col.2, line 56). Fernando was directed to the execution of the flag-modifying instructions in a different number of clocks (e.g. see col.1,lines 51-56), therefore, it is a sequence processor.

13. As to claims 32, 33, Fernando also conditionally executing in a sequence processor and based on a complex condition (see branch on true condition and the condition extensions see col.5, lines 6-15).

14. As to claim 58, 68, Fernando also included at least zero indication.

15. As to claim 67, Fernando's first instruction was also a compare instruction. (see col.2, line 55 CMP).

16. As to claim 70, Fernando's second instruction was also directed to selectable conditional bit (see the true or false condition in col.5, lines 7-20).

17. As to claims 60, 64, Fernando disclosed at least :

- a) setting scalar flags [flag bit in PSW] based on at least one side effect of execution of a first instruction [CMP] (col.2, line 55)
- b) setting arithmetic condition flags (BRA.iff , see if true and if not true in col.5, lines 7-20) based on arithmetic scalar flag [r1=0,1] as specified by the first instruction [CMP];
- c) determining whether to execute a second instruction based on the state of the arithmetic condition flags (see BRA.iff in col.2, lines 56)
- d) executing the second instruction (see the execution ADD in col.2, line 57, see also the jump and add sub instructions in col.5, lines 7-20);
- e) Fernando's second instruction was also directed to selectable conditional bit (see the true or false condition in col.5, lines 7-20).

18. Fernando did not specifically show his scalar flags (see the flag in PSW) were arithmetic flags as claimed. However, Okayama disclosed clearly a PSW for storing arithmetic flags (see the fig. PSW for storing overflow , carry). It would have been obvious to one of ordinary skill the art to use Okayama in Fernando for including the arithmetic flags into the PSW because the use of Okayama could expand the

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capability of Fernando to adapt to specific application of the processor, such as the arithmetic conditional flags resulted from the arithmetic unit, and because Fernando also taught the flag in his PSW was modified by arithmetic instructions (see the flag modified by the multiply or division instructions in col.4, lines 57-67, col.5, lines 1-56), therefore one of ordinary skill in the art should be able to recognize the PSW of Fernando should be applicable for using the arithmetic flags in order to enhance the processing ability of the system ,and in doing so , provided a motivation.

19. As to claim 61, Fernando also included combinatorial logic (see the background of combinatorial logic circuit in col.2, lines 1-11).

17. As to claim 62, Fernando's second instruction also effect arithmetic scalar flags (see ADD instruction).

20. AS to claim 73, Fernando disclosed at least :

- a) storage device for storing arithmetic flags (see PSW register in col.4, lines 35-56);
- b) execution unit for executing a first instruction [CMP], generating condition state [Flag] as a side effect [result] of the execution (e.g. see first instruction and the flag bit in col.2, line 55, see the storage of the flag in col.4, lines 35-56) ;
- c) generating unit for receiving condition state , generating condition flag (see the setting of the flag in col.4, lines 63-65) utilizing both the condition state [flag] and opcode bit [extension .eq0] (see col.2, lines 55-56, see col.5, lines 7-20 for determination of the true or false condition) and an opcode bit [.eq] from the first instruction, storing condition flag I the storage device [PSW] ;

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d) conditionally executing a second instruction [Add] based on the state of the condition flag (see the instruction ADD executed if true, in col.2, lines 56-57).

21. Fernando did not specifically show his set of condition flags (see the PSW) was arithmetic flags as claimed. However, Okayama disclosed clearly a PSW for storing arithmetic flags (see the fig. PSW for storing overflow , carry). It would have been obvious to one of ordinary skill the art to use Okayama in Fernando for including the arithmetic flags into the PSW. The reasons of obviousness were already given in the paragraph , therefore, it will not be repeated herein.

22. As to claim 74, Fernando's first instruction was also a compare instruction. (see col.2, line 55 CMP).

23. As to claim 75, Fernando also included at least zero indication.

24. As to claim 77, Fernando also included selectable condition opcode bit (see the .ift in col.5, lines 7-20).

25. As to claim 78, Fernando also included combinatorial logic (see the background of combinatorial logic circuit in col.2, lines 1-11).

26. As to claim 79, Fernando's second instruction also effect arithmetic scalar flags (see ADD instruction).

27. Claim 63 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the operation performed by the first instruction on packed data comprising a plurality of data elements , setting one arithmetic flag for each data element of the packed data.

28. Claim 65 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the execution of the first instruction by first processing element and the conditionally execution of the second instruction by a second processing element.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

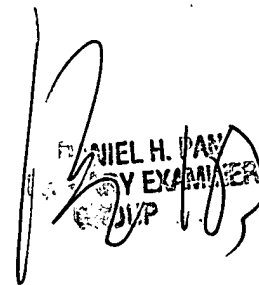
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162.

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The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan


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